REMARKS

After entry of this Amendment, claims 4-13, 18, 19, 21-24, 31-42, 44-46, and 51-71 will be pending in this application; claims 74-76 have been cancelled; claims 4, 5, 31-37, 40, 44-46, 51, 55, 57, 61, 63, 67 have been amended. Support for the amendments may be found throughout the Specification, at least in Figures 3 and 13 and related text, in the originally filed claims, and on page 26, line 21 to page 27, line 3 of the clean version of the Specification submitted with the Response to Office action dated November 17, 2006.

Objections to Claims

Claims 31, 36, 37, 39, 44, 46, 57, and 63 are objected to for informalities. Applicants respectfully submit that the foregoing amendments fully address the objections to these claims.

Rejection of Claims under 35 U.S.C. § 112

Claims 4-13, 18, 19, 21-24, 31-42, 44-46, and 51-71 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicants respectfully submit that the foregoing amendments fully address these rejections.

Rejection of Claims under 35 U.S.C. § 102

Claims 4-7, 11-13, 18, 19, 21, 22, 31-42, 44-46, and 51-71 are rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 4,661,927 to Graebel ("Graebel"). Graebel appears to disclose a Schottky logic read only memory. *See* Graebel, abstract. The Examiner relies on Graebel to teach all of the limitations of independent claim 31.

Graebel does not, however, disclose *address circuitry comprising a first pattern of rectifiers connected directly to a first set of conductive lines*, as recited in independent claim 31. The Examiner states that Graebel's Y address buffer/decoder 16 and sense amplifier 20 (including example sense amplifier 100) are address circuitry. However, sense amplifier 100, including diodes 102-108, is not address circuitry. Rather, sense amplifier 100 "provides an output on line 124 which is a function of the state of the bit stored at the intersection of the selected wordline with one of the four bitlines which is selected by Y address buffer/decoder 16."

See Graebel, column 5, lines 21-25 (emphasis added). Only Y address buffer/decoder 16, in which NPN transistors and PNP clamps are connected directly to Y decoder lines Y0-Y3, functions as address circuitry by selecting particular bitlines. *See* Graebel, Fig. 5 and related text. In contrast, sense amplifier 100 merely provides an output determined by the presence or absence of a diode connecting the bitline and wordline selected by Y address buffer/decoder 16 and wordline decoder/drivers 14, and hence performs no addressing function. *See* Graebel, column 5, lines 21-40. Hence, Graebel does not teach or suggest address circuitry comprising a first pattern of rectifiers connected directly to a first set of conductive lines, as recited in independent claim 31.

Applicants submit that amended independent claim 31 and claims dependent therefrom are allowable for at least this reason.

CONCLUSION

In light of the foregoing, Applicants respectfully submit that all claims are now in condition for allowance.

Applicants believe that no additional fees are necessitated by the present Response. However, in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Deposit Account No. 07-1700.

If the Examiner believes that a telephone conversation with Applicants' agent would expedite allowance of this application, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,

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